REMARKS

This paper is responsive to the Office Action mailed from the Patent and Trademark Office on November 18, 2002, which has a shortened statutory period set to expire February 18, 2003.

Drawings

The drawings are objected to on page 2 of the Office Action.

In the appended "redline" sheet, Fig. 3 is amended to exchange the lead line destinations for reference numbers 346 and 348. No new matter is introduced in either of the above amendments. Reconsideration and withdrawal of these objections is respectfully requested.

The "redline" sheet and a replacement sheet including the above-mentioned amended Fig. 3 are entered under the Submission of Proposed Drawing Amendment, which is submitted with this paper.

Claims

Claims 1-10 are pending in the above-identified application. Claims 1-10 are rejected under 35 USC 103 as being unpatentable over cited references that are identified below.

In the current paper, originally-filed Claims 1, 2 and 8 are amended, and Claims 21-30 are newly entered. Claims 3-7, 9 and 10 remain as filed. No new matter is entered. Reconsideration and withdrawal of the pending rejections in view of the following remarks is respectfully requested.

Amendment to Claim 1

Claim 1 is amended herein to recite (in pertinent part):

> ... wherein each air-gap extends from a top surface of a corresponding second line to a bottom surface of said each first line.

The above-quoted language is clearly supported in Applicants' Figs. 3 and 4(D). Note that, in the sequence illustrated in Applicants' Figs. 4(A) through 4(D) and described in Applicants' specification (i.e., paragraphs 0026 through 0030), a gate line 125 is formed on the upper surface of a substrate 400 (paragraph 0026), then a release material 410 is formed over the gate line 125 (paragraph 0027), then a data line 130 is formed on the release material 410 (paragraph 0029). Finally, as indicated in Applicants' Figs. 4(C) and 4(D) (reproduced below for reference), the release material 410 is etched to form an air-gap 302 extending between an upper surface of gate line 125 and a lower surface of data line 130:

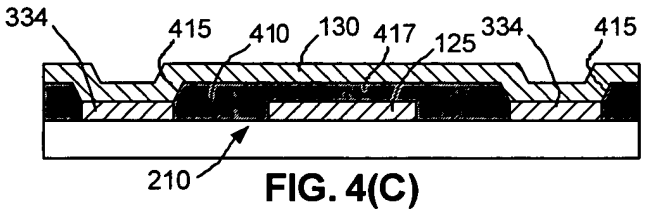

FIG. 4(C)

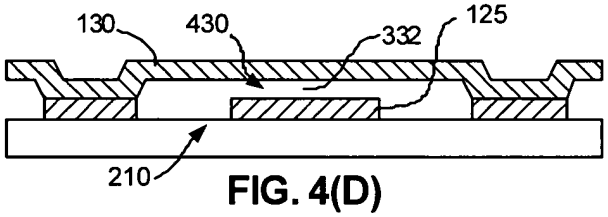

FIG. 4(D)

Fig. 4(D) shows a subsequent release (etch) process during which release material is etched using a suitable etchant 430 in a manner that does not significantly damage data lines 130 and gate lines 125. Accordingly, release material portion 417 (see Fig. 4(C) is removed from crossover location 210 such that an air-gap 302 is defined between data line 130 and gate line 125. (Paragraph 0030.)

Amendment to Claim 2

Claim 2 is amended to correct an obvious typographical error. No new matter is entered.

Amendment to Claim 8

Similar to the amendment to Claim 1, Claim 8 is amended to recite "wherein an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines such that each air-gap extends from a top surface of a

corresponding gate line to a bottom surface of said each data line." Support for this amendment is essentially identical to that described above with reference to Claim 1.

Rejection Under 35 USC 103

Claims 1-3 and 6

Claims 1-3 and 6 are rejected under 35 USC 103 as being unpatentable over Kingsley (USP 5,587,591, herein "Kingsley") in view of Kunikiyo (USPUB 2002/0135041, herein "Kuniyoko").

In rejecting Claim 1, the Examiner states (in pertinent part):

> Kunikiyo teaches in figures 12 and 13, and paragraph 0119 wherein an air-gap (200) is defined at each crossover location that separates a first line (53) form the plurality of second lines (52).

As amended, Claim 1 is believed to be distinguished over Kingsley and Kunikiyo in that neither of these references teach or suggest an "air-gap" that "extends from a top surface of a corresponding second line to a bottom surface of said each first line", as recited in Claim 1. In particular, Kingsley fails to disclose any type of "air-gap" structure. Further, Kunikiyo discloses a crossover structure defining an air-filled layer space 200 that is located between an upper line 53 and a lower line 52. Although Kunikiyo is difficult to interpret, Applicants believe that air-filled layer space 200 does not extend from "a top surface of a corresponding gate line to a bottom surface of said each data line", as recited in Claim 1. Instead, Applicant interpret the last sentence of paragraph 0118 to indicate that a boron phosphosilicate glass (BPSG) bridge structure may be formed between upper line 53 and lower line 52. For reference, the last line of paragraph 0118 teaches "While the trench 60 is provided to form the cavity 57 as will be

described below, it is flattened by the BPSG film 59 so that a wiring layer or the like can further be formed thereon." Applicants understand this passage to mean that a BPSG bridge structure that is similar to "BPSG 44" (shown most clearly in Kuniyoko's Fig. 9) may be formed before upper line 53 is formed.

Based on the apparent teachings of Kunikiyo (provided above), and because Kunikiyo fails to teach or suggest a method for forming an air-gap "such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line", as recited in amended Claim 1, it would have been neither possible nor obvious to combine the teachings of Kingsley and Kunikiyo to produce the structure recited in Claim 1.

Further, Applicant respectfully traverses this rejection because, due to their very different subject matter, it would not have been obvious to combine the teachings of Kunikiyo with the solid state fluoroscopic radiation imager of Kingsley. In particular, Kingsley's radiation imager includes a "large area photosensor array" (abstract), and Kunikiyo is clearly directed to a "conventional" semiconductor integrated circuit. Those of ordinary skill in the art will recognize that the fabrication techniques associated with the formation of large area photosensor arrays are quite different from those utilized to fabricate conventional semiconductor integrated circuits. Therefore, it would not have been obvious to utilize the specialized techniques taught by Kunikiyo to produce the large area photosensor array of Kingsley.

Claims 2, 3 and 6 are dependent from Claim 1, and are therefore distinguished over the cited prior art for at least the same reasons as those set forth with respect to Claim 1.

Claim 4

Claim 4 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Kunikiyo, and further in view of Akiyama (USP 5,712,494, herein "Akiyama").

Claim 4 is dependent from Claim 1, and is therefore distinguished over Kingsley and Kunikiyo for at least the same reasons as those set forth above with respect to Claim 1. Further, Akiyama fails to overcome the deficiencies of Kingsley and Kunikiyo. Therefore, Claim 4 is distinguished over the cited prior art for reasons similar to those set forth above with respect to Claim 1.

Claim 5

Claim 5 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Kunikiyo, and further in view of Hwang (USP 6,337,284, herein "Hwang").

Claim 5 is dependent from Claim 1, and is therefore distinguished over Kingsley and Kunikiyo for at least the same reasons as those set forth above with respect to Claim 1. Further, Hwang fails to overcome the deficiencies of Kingsley and Kunikiyo. Therefore, Claim 5 is distinguished over the cited prior art for reasons similar to those set forth above with respect to Claim 1.

Claim 7

Claim 7 is rejected under 35 USC 103 as being unpatentable over Kingsley in view of Kunikiyo, and further in view of Street (USP 5,789,737, herein "Street").

Claim 7 is dependent from Claim 1, and is therefore distinguished over Kingsley and Kunikiyo for at least the same reasons as those set forth above with respect to Claim 1. Further, Street fails to overcome the deficiencies of Kingsley and Kunikiyo. Therefore, Claim 7 is distinguished over the

cited prior art for reasons similar to those set forth above with respect to Claim 1.

Claim 8 and 10

Claims 8 and 10 are rejected under 35 USC 103 as being unpatentable over Fukuda in view of Kunikiyo. Similar to the rejection of Claim 1, in rejecting Claim 8, the Examiner relies on Kunikiyo's teaching of the "air-gap" (200):

> Kunikiyo teaches in figures 12 and 13, and paragraph 0119 wherein an air-gap (200) is defined at each crossover location that separates a first line (53) form the plurality of second lines (52).

As amended, Claim 8 is believed to be distinguished over Fukuda and Kunikiyo in that neither of these references teach or suggest an "air-gap" that "extends from a top surface of a corresponding second line to a bottom surface of said each first line", as recited in Claim 1. In particular, Fukuda fails to disclose any type of "air-gap" structure. Further, as set forth above in response to the rejection of Claim 1, Kunikiyo fails to teach or suggest a method for forming an air-gap "such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line", as recited in amended Claim 8. Therefore, it would have been neither possible nor obvious to combine the teachings of Fukuda and Kunikiyo to produce the structure recited in Claim 8.

Claim 9

Claim 9 is rejected under 35 USC 103 as being unpatentable over Fukuda in view of Kunikiyo, and further in view of Antonuk (USP 5,262,649, herein "Antonuk").

Claim 9 is dependent from Claim 8, and is therefore distinguished over Fududa and Kunikiyo for at least the same

reasons as those set forth above with respect to Claim 8. Further, Antonuk fails to overcome the deficiencies of Fududa and Kunikiyo. Therefore, Claim 9 is distinguished over the cited prior art for reasons similar to those set forth above with respect to Claim 8.

For the above reason, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 USC 103.

New Claims 21-30

Claims 21-30 are newly entered.

Claims 21 through 27 are dependent from Claim 8, and are therefore distinguished over the cited prior art for at least the same reasons as those set forth with respect to Claim 8.

Similar to Claims 1 and 8, new Claim 28 recites (in part):

> ... a plurality of first lines, each first line being formed on the upper surface of the substrate and connected to a corresponding first group of said pixel circuits; and
>
> a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:
>
> each second line including:
>
> first portions supported by the upper surface of the substrate, and
>
> second portions extending over the plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line.

Therefore, new Claim 28 is believed to be distinguished over the cited prior art at least for reasons similar to those provided above with reference to Claims 1-10.

Claim 29 is dependent from Claim 28, and is therefore distinguished over the cited prior art for at least the same reasons as those set forth with respect to Claim 28.

Finally, support for Claim 30 is indicated below with reference to Fig. 4(D).

30. (New) An image sensor array comprising:
a substrate having an upper surface defining a plane;
a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;
a plurality of first lines, each first line being formed over the upper surface of the substrate and connected to a corresponding first group of said pixel circuits;
a plurality of support pads, each support pad being formed over the upper surface of the substrate; and
a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:
a plurality of first portions, each first portion contacting a corresponding support pad, and
second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion.

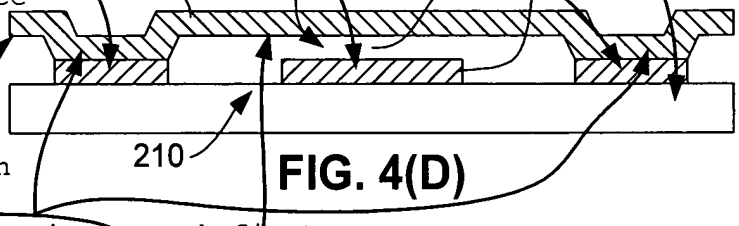

FIG. 4(D)

For the above reasons, Applicants believe Claims 1-10 and 21-30 are in condition for allowance. Should the Examiner have any questions regarding the present paper, the Examiner is invited to contact the undersigned attorney at the number provided below.

CONCLUSION

Claims 1-10 and 21-30 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. Attached is a marked-up version showing the amendments in a document entitled "VERSION WITH MARKINGS TO SHOW CHANGES MADE". If there are any questions, please telephone the undersigned at (408) 451-5902 to expedite prosecution of this case.

Respectfully submitted,

Customer No.: 28014
Telephone: (408) 451-5902

Patrick T. Bever
Attorney for Applicant
Reg. No. 33,834

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on February 3, 2003.

Feb 3, 2003 _____
Date Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

DRAWINGS

(See attached "redline" copy of Fig. 3 showing changes.)

CLAIMS

Please amend Claims 1, 2, and 8 as follows:

1. (Amended) An integrated circuit comprising:

a plurality of pixel circuits arranged in rows and columns;

a plurality of first lines, each first line connected to a corresponding column of pixel circuits; and

a plurality of second lines, each second line connected to a corresponding row of pixel circuits,

wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each first line from the plurality of second lines, wherein each air-gap extends from a top surface of a corresponding second line to a bottom surface of said each first line.

2. (Amended) The integrated circuit according to Claim 1, wherein each pixel circuit includes an access transistor and a pixel element, wherein the access transistor includes a gate terminal connected to [and] an associated first line, a first terminal connected to the pixel element, and a second terminal connected to an associated second line.

8. (Amended) An image sensor array comprising:

a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor;

a plurality of gate lines, each gate line connected to the

access transistors of a corresponding column of pixel circuits; and

a plurality of data lines, each data line connected to the access transistors of a corresponding row of pixel circuits,

wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line.

Please enter new Claims 21-30 as follows:

21. (New) The image sensor array according to Claim 8, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

22. (New) The image sensor array according to Claim 21, wherein the self-aligned thin-film transistor of each pixel circuit comprises:

an amorphous silicon (a-Si:H) layer including a relatively undoped first region located over an associated gate line, the first region being located between a doped second region and a doped third region; and

an optical filter island located over the first region, the optical filter island comprising at least three layers having at least two indexes of refraction and being arranged such that the optical filter island is reflective of a first radiation wavelength and transmissive of a second radiation wavelength.

23. (New) The image sensor array according to Claim 22,

wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate,

wherein the metal plate is connected to the doped second region of the self-aligned thin-film transistor, and

wherein an associated data line is connected to the doped third region of the self-aligned thin-film transistor.

24. (New) The image sensor array according to Claim 8, wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated data line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

25. (New) The image sensor array according to Claim 24, wherein the buried insulator layer has a thickness of 3 to 5 microns.

26. (New) The image sensor array according to Claim 24, wherein the charge sensing region of each of the plurality of pixel circuits comprises an amorphous silicon (a-Si:H) layer.

27. (New) The image sensor array according to Claim 8,

wherein the image sensor array further comprises spaced-apart data line support pads formed from the first metal layer, and

wherein each spaced-apart data line support pad contacts an associated data line.

28. (New) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns

over the upper surface of the substrate;

a plurality of first lines, each first line being formed on the upper surface of the substrate and connected to a corresponding first group of said pixel circuits; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

first portions supported by the upper surface of the substrate, and

second portions extending over the plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line.

29. (New) The image sensor array according to Claim 28, further comprising a plurality of support pads, each support pad being formed on the upper surface of the substrate and contacting a corresponding first portion of an associated second line.

30. (New) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;

a plurality of first lines, each first line being formed over the upper surface of the substrate and connected to a corresponding first group of said pixel circuits;

a plurality of support pads, each support pad being formed over the upper surface of the substrate; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

a plurality of first portions, each first portion

contacting a corresponding support pad, and

second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion.